REMARKS

Applicant thanks the Examiner for the thorough consideration given the present application. Claims 11-18 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the Amendments and Remarks as set forth hereinbelow.

CLAIM FOR PRIORITY

It is gratefully acknowledged that the Examiner has recognized the Applicant's claim for foreign priority. Because the Applicant's claim for priority has been perfected, no additional action is required from the Applicant at this time.

DRAWINGS

It is gratefully acknowledged that the Examiner has approved the Formal Drawings submitted by the Applicants. The drawings comply with the requirements of the USPTO. No further action is necessary.

ACKNOWLEDGEMENT OF INFORMATION DISCLOSURE STATEMENT

The Examiner has acknowledged the previously filed Information Disclosure Statement. An initialed copy of the PTO-1449 has been received from the Examiner. No further action is necessary at this time.

SPECIFICATION CHANGES

The specification has been amended to correct minor informalities. No new matter has been added.

REJECTION UNDER 35 U.S.C § 112

Claims 1-10 stand rejected under 35 U.S.C. § 112. This rejection is respectfully traversed.

Claims 1-10 have been cancelled and have been replaced by new claims 11-18. Accordingly, this rejection is moot. In addition, new claims 11-18 have been drafted to be definite within the meaning of 35 U.S.C. § 112, second paragraph.

REJECTION UNDER 35 U.S.C § 102

Claims 1-7 and 9 stand rejected under 35 U.S.C § 102 as anticipated by Hayashi et al. This rejection is respectfully traversed.

As discussed above, claims 1-10 has been cancelled. Accordingly, comments will be presented distinguishing new claims 11-18 over Hayashi et al.

In more detail, new independent claim 11 is directed to a method of manufacturing a substrate for a semiconductor substrate. The method includes forming connection terminals on a first surface of the substrate, in which the first surface corresponding to a surface on which a semiconductor element is to be mount, and

counterboring a second surface of the substrate that is opposite to the first surface using a cutting blade until the cutting blade contacts the connection terminals so as to expose the connection terminals and form a circuit component mounting hole.

These features are supported at least by Figs. 3A and 4A and corresponding description of this specification. For example, Fig. 3A illustrates forming connection terminals 23a on a first surface of the substrate 20, in which the first surface corresponds to a surface on which a semiconductor element 10 is to be mounted. In addition, Fig. 4A illustrates counterboring a second surface of the substrate20 that is opposite to the first surface using a cutting blade until the cutting blade contacts the connection terminals 23a so as to expose the connection terminals 23a and form a circuit component mounting hole 32.

On the contrary, as shown in Figs. 2(A) and Fig. 4(A) in Hayashi et al., the component mounting hole 5c is drilled all the way through the substrate, a circuit component is mounted in

the component mounting hole 5c and the gaps in the component mounting hole are filled. Then, Hayashi et al. forms cable layers on both sides of the substrate. As shown in Fig. 4(A), the substrate is not counterbored until the connection terminals 38a are exposed.

Accordingly, it is respectfully submitted independent claim 11 and each claim depending therefrom patentably define over Hayashi et al.

REJECTION UNDER 35 U.S.C. § 103

Claims 8 and 10 stand rejected under 35 U.S.C. § 103 as unpatentable over Hayashi et al. in view of Mak et al. This rejection is respectfully traversed.

It is respectfully submitted this rejection has also been overcome as Mak et al. also does not teach or suggest the features recited in new independent claim 11.

CONCLUSION

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone David A. Bilodeau at (703) 205-8072 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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